CLAIMS:

1. A frequency divider comprising:

- a first flip-flop (M1, M2, M3, M4) having a first clock input ($\overline{Ci}$) for receiving a clock signal, the flip-flop further comprising a first set input (Q4) and a first non-inverted output (Q1), and

- a second flip-flop (M1', M2', M3', M4') having a second clock input (Cl) for receiving a second clock signal that is substantially in anti-phase with the clock signal inputted into the first clock input ($\overline{Ci}$), a second set input coupled to the first non-inverted output (Q1), a second non-inverted output (Q2) and a second inverted output ($\overline{Q2}$), the second inverted output ($\overline{Q2}$) being coupled to the first set input (Q4).

2. A frequency divider as claimed in Claim 1, wherein a period of the clock signal is of the same order of magnitude as a delay through an inverter stage of the divider.

3. A frequency divider as claimed in Claim 1, wherein a controllable switch (M7) is coupled to the first data input (Q4) and to the third output (Qa2) and being controlled by a clock signal driving the first flip-flop (M1, M2, M3, M4).

4. A frequency divider as claimed in Claim 1, wherein the controllable switch (M7) is coupled to the third output (Qa2) via resistive means (R).